G 1535 (Pages : 2) Reg. No.:.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Fourth Semester

Branch : Applied Electronics and Instrumentation/Electronics and Communication/Electronics and Instrumentation/Instrumentation and Control Engineering

AI 010 404/EC 010 404/EI 010 404/IC 010 404—DIGITAL ELECTRONICS (AI, EC, EI, IC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Explain the properties of Error correcting and detecting codes. Mention their applications.
2. Define and explain : (1) Propagation delay ; (2) Fan in ; and (3) Emitter coupled logic.
3. What is the difference between combinational logic and sequential logic circuits ? Explain.
4. Mention the potential applications of counters. Explain any *two* in detail.
5. Draw the block diagram of PLA and explain it.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. State and explain Demorgan's theorem.
7. Explain the subfamilies of CMOS in detail.
8. Differentiate latch from FFs. Explain the difference.
9. Explain the types of ROM in detail.
10. Differentiate Static Hazard from Dynamic Hazard. Explain the difference.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (i) Explain : (1) BCD ; (2) XS 3 code with examples.

    (ii) Explain Binary and octal number systems with examples.

Or

Turn over

12. (i) Explain the limitation of K map.

(ii) State and prove all the Boolean law's.

13. (i) Explain positive and negative logics in detail.

(ii) Draw a basic ECL inverter and explain it in detail.

Or

14. Explain the characteristics of TTL and CMOS logic families, NMOS NOR gate in detail.

15. Explain the half and full subtractors with schematic diagrams. Realize them with basic gates.

Or

16. (i) Explain the all the types of FFs with diagrams, truth tables and excitation tables.

(ii) Derive the characteristic equations of all the types of FFs.

17. Explain the design steps of MOD n synchronous counter with an example.

Or

18. (i) Explain the types of shift register with neat diagrams.

(ii) Give an account on "Universal Register".

19. (i) Explain the steps to design a hazard free combinational circuit with an example.

(ii) Draw the architecture of CPLD and explain in detail.

Or

20. (i) Draw the architecture of FPGA and explain it in detail.

(ii) Write a technical note on "ASIC-categories".

(5 × 12 = 60 marks)