F 3636 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Fifth Semester

Branch : Electronics and Communication Engineering

EC 010 503—DIGITAL SYSTEM DESIGN (EC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Define operators. List out the different types of operators.
2. Differentiate ROM and PLA ?
3. Define FSM ? Draw the block diagram of FSM.
4. List out the ASM chart components.
5. Define linear feedback shift register.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Implement de–multiplexer using verilog.
7. Describe the typical ROM internal origination with neat diagram.
8. Explain Meta stability.
9. Write a short note on algorithmic state machine.
10. Write a Verilog code for up/down counter.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Write a short note on :
    (i) Signal drivers.
    (ii) Data types.
    (iii) Language elements.

Or

12. Design an encoder using two half adders by writing Verilog program.

13. Design using PLA the following Boolean functions.

    (i) $X(A, B, C) = \sum (0, 1, 2, 4)$

    (ii) $Y(A, B, C) = \sum (0, 5, 6, 7)$.

Or

14. Explain Quine–McCluskey algorithm in detail.

15. Design a sequence detector which detects the sequence "01110" using D flip–flops.

Or

16. Design a serial binary adder using delay flip–flops.

17. Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected using ASM chart.

Or

18. Explain state assignments in detail.

19. What is barrel shifter ? Explain its principle. Using Verilog HDL, Model a 4–bit parallel shifter.

Or

20. Write a note on :

    (i) FSM.

    (ii) Linear feedback shift register.

(5 × 12 = 60 marks)