G 1224 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Sixth Semester

Branch : Electronics and Communication Engineering

EC 010 604—COMPUTER ARCHITECTURE AND PARALLEL PROCESSING (EC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Define zero-address, one-address and 1½ address instructions.
2. Explain how floating point numbers are represented.
3. What is meant by locality of reference ?
4. Write a note on data dependences.
5. List the functions of SMPS.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Briefly explain program controlled I/O.
7. Explain single bus, two bus and three bus structures.
8. Write a note on I/O channels.
9. Explain Flynn's classification of computers.
10. Write a note on Pentium processor.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Explain various addressing modes.

Or

12. Write a note on pipelining. Explain multithreading.

Turn over

13. Explain hardwired and microprogrammed control.

Or

14. Explain restoring division and non-restoring division algorithms.

15. Explain various semiconductor RAM memories.

Or

16. Give the block diagram showing memory organization of a 4 M × 16 memory using 256 K × 1 memory chips.

17. Explain message passing architecture.

Or

18. Write notes on multicore processors, multiprocessor systems and multicomputer systems.

19. Explain the architecture of a PC, with block diagram.

Or

20. Explain the architecture and components of motherboard.

(5 × 12 = 60 marks)