G 705   (Pages : 2)   Reg. No....................................

Name....................................

B.TECH. DEGREE EXAMINATION, MAY 2014

Seventh Semester

Branch : Electronics and Communication Engineering

EC 010 701—VLSI DESIGN (EC)

(Improvement/Supplementary)

[2010 admissions]

Time : Three Hours   Maximum : 100 Marks

Part A

Answer all questions.

Each question carries 3 marks.

1. Discuss the need for an epitaxial layer.

2. Write a note on vias.

3. Discuss the features of CPL.

4. Explain the features of BiCMOS Technology.

5. Explain the advantages of the use of FPGA in IC design.

                                                             (5 × 3 = 15 marks)

Part B

Answer all questions.

Each question carries 5 marks.

6. Write a note on metallization.

7. Explain the advantages of Si gate technology.

8. Explain latchup in CMOS.

9. Explain how the electrical and physical parameters of CMOS transistor vary with scaling.

10. Explain channeling effect.

                                                             (5 × 5 = 25 marks)

Part C

Answer all questions.

Each question carries 12 marks.

11. Explain Czochralski process. Give the features of Cz grown Si.   (12 marks)

Or

12. Explain the process of ion implantation.   (12 marks)

13. Explain the different techniques used in the isolation of components in IC fabrication.

(12 marks)

Or

14. Explain the design of monolithic resistors and capacitors.   (12 marks)

15. Discuss the implementation of a XOR gate using CMOS logic. Implement the same using TG. Compare them.

(12 marks)

Or

16. Explain stick diagrams and their use in IC layout. Draw the stick diagram of a two input NAND gate.   (12 marks)

17. (a) Explain the implementation of JKFF using CMOS logic.   (6 marks)

    (b) Explain the concept of scaling. Can this be directly implemented in practice. If Yes/No explain.

(6 marks)

Or

18. (a) Explain the structure of BiCMOS two input NOR gate. Compare it with its CMOS counterpart.

(7 marks)

    (b) Explain the VI characteristics of a CMOS inverter.   (5 marks)

19. (a) Explain the doping process of a GaAs crystal.   (7 marks)

    (b) Write a note on PLDs.   (5 marks)

Or

20. (a) Explain the crystal structure of GaAs.   (7 marks)

    (b) Compare Si and GaAs technologies.   (5 marks)

[5 × 12 = 60 marks]