G 1039 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Seventh Semester

Branch : Electronics and Communication Engineering

EC 010 701—VLSI DESIGN (EC)

(New Scheme—2010 Admission onwards)

[Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. List the process steps used in IC fabrication.
2. List the difference between PMOS and NMOS.
3. Draw the stick diagram for NOT gate.
4. Draw the Bi-CMOS layout structure.
5. List the difference between ASIC *vs*. FPGA.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Write a note on chemical vapour deposition.
7. Describe Junction isolation and Dielectric isolation.
8. With neat CMOS structure explain latch up in CMOS.
9. Realize the following Boolean equation using transmission gates : $f = ab + abc$.
10. Design NOR gate using CMOS technique and draw the stick diagram for the same.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. With neat diagram, explain X-ray lithography.

Or

12. Elaborate with each and every steps of NMOS IC fabrication flow.

Turn over

13. Explain monolithic diodes and Schottky diodes with neat figure.

Or

14. Describe NMOS enhancement mode operation along with its characteristic curve.

15. With neat figure, explain each and every fabrication steps of CMOS Technology.

Or

16. Design and explain NOR-4-bit shifter.

17. With neat figure, explain CMOS sequential SR flip-flop and JK flip-flop.

Or

18. Discuss about BiCMOS Technology.

19. Describe about GaAs fabrication Technology.

Or

20. Write a short note on :

    (a) PLA.

    (b) FPGA.

(5 × 12 = 60 marks)