

B.TECH. DEGREE EXAMINATION, APRIL 2011**Fourth Semester**

Branch : Computer Science and Engineering

COMPUTER ORGANIZATION (R)

(Regular/Improvement/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Part A*Answer all questions.**Each question carries 4 marks.*

1. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers :
 - (i) How many selection inputs are there in each multiplexer?
 - (ii) How many multiplexers are there in the bus?
2. Explain the stored program concept.
3. Explain bit sliced ALU.
4. Compare and contrast serial and parallel adders.
5. Explain how a micro-instruction is executed in vertical approach.
6. Explain hardwired control.
7. Define and explain associative memory.
8. Explain the terms : (a) Cache hit ; and (b) Cache miss.
9. Explain the working principle of an optical mouse.
10. Describe the GPIB standard.

(10 × 4 = 40 marks)

Part B*Answer either Section (a) or (b) of each module.**Each full question carries 12 marks.***MODULE 1**

11. (a) With a neat diagram, describe how the CPU, memory and control units in a digital computer interact.

Or

- (b) Describe the different bus structure and their organisations in a digital computer.

Turn over

MODULE 2

12. (a) With a neat circuit diagram, explain how a two-level carry look ahead adder helps in improving the speed of addition.

Or

- (b) With neat diagrams, describe the behaviour and structure of restoring division scheme with 2's complement members.

MODULE 3

13. (a) Draw and explain the organisation of nano program control. Compare the single level and two level controls.

Or

- (b) With a neat flow chart, explain the fetch and execution cycle on the data path of a CPU.

MODULE 4

14. (a) Give the complete design of a $4\text{ K} \times 8$ memory module built out of 32×32 static MOS cell array chip with in-built decoders.

- (i) Draw the block diagram of the memory module with the chip as the building block.
- (ii) Also draw the internal block diagram of the chip and number of pins necessary on the chip.

Or

- (b) Draw and explain a 3×2 associative memory. Explain how read/write operations are accomplished?

MODULE 5

15. (a) Describe the principle of operation of a VDU terminal specifying the RTL structure to control its operation.

Or

- (b) (i) What are graphic input-output devices? Explain any *two* each, bringing out their special features.
- (ii) Compare and contrast DMA and IO interrupt I/O transfer schemes.

(8 + 4 = 12 marks)

[5 × 12 = 60 marks]