F 9366   (Pages : 3)   Reg. No................................

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B.TECH. DEGREE EXAMINATION, NOVEMBER 2011

Fourth Semester

Branch : Computer Science and Engineering

ADVANCED MICROPROCESSORS AND PERIPHERALS (R)

(2002 admission onwards—Supplementary)

Time : Three Hours   Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 marks.

1. Write the control word for the following configuration of the ports of 8255 for mode 2 operation :

    Port A – bidirectional, Mode of Port A – mode 2

    Port B – input, mode of Port B – mode 0.

2. Explain the handshaking mode of operation.

3. Distinguish between programmed data transfer and interrupt driven data transfer.

4. Explain how will you design a programmable sample rate generator for A/D subsystem ?

5. What is pipelined architecture ? How it is implemented in 8086 ?

6. Mention any four addressing modes in 8086. Give examples for each.

7. Explain the effect of the following instructions of 8086 :—

    (i)   AAM.   (ii) LEA Si, X.

    (iii) PUSH F.   (iv) CMP.

8. Explain real and protected modes in 80286.

9. Explain the circuit for generating memory and I/O control signal for 80386.

10. Explain the address space of PENTIUM III.

                                                            (10 × 4 = 40 marks)

Part B

Answer any **one** *full question from each module.*
Each full question carries 12 marks.

Module 1

11. Explain different methods of data communication and architectural features of 8251.

Or

12. With neat diagrams, explain the various features of 8252. Show how it is interfaced with 8085 ?

Module 2

13. Interface an 8-bit ADC with 8085 using memory mapped I/O. Also write an interrupt routine to read the output data of the converter, store it in memory and continue to collect data for the specified "n" number of times.

Or

14. Assume that 8255 control register and ports are assigned below as :

        CR – 9003 H

        PA – 9000 H

        PB – 9001 H

        PC – 9002 H

Design and draw a system with 8255 port connection to read the status of 8 switches and displays the compliments of that in another 8 LED's. Write the program for the same.

Module 3

15. (a) Explain the maximum mode configuration and timing diagram of 8086 system.

    (b) Draw and explain the read cycle timing diagram for minimum mode of 8086.

                                   (8 + 4 = 12 marks)

Or

16. (a) Explain the register organisation of 8086 ?

    (b) Explain the memory segmentation of 8086. What are its advantages ?

                                   (6 + 6 = 12 marks)

Module 4

17. (a) Explain the machine language instruction formats followed in 8086.   (6 marks)

    (b) Write an Assembly Language Program to find out the largest number from an unordered array of sixteen 8-bit numbers stored sequentially in the memory locations starting at offset 0400H the segment 2000 H.

                                   (6 marks)

Or

18. (a) Write an Assembly language program to reverse the given string of 10 characters stored in the memory DS : 2000 H, store the reverse pattern in DS : 4000 H.

                                   (8 marks)

    (b) What do you mean by interrupt priorities ? List out the interrupt priorities in 8086.

                                   (4 marks)

Module 5

19. (a) List and explain different data types supported by 80386 ?   (6 marks)

    (b) Write a note on descriptors and descriptor tables.   (6 marks)

Or

20. With a neat block diagram, explain the PENTIUM CPU architecture and also explain the super scalar organisation.

(12 marks)

[5 × 12 = 60 marks]