G 515 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Applied Electronics and Instrumentation/Electronics and Communication/Electronics and Instrumentation/Instrumentation and Control Engineering

AI 010 404/EC 010 404/EI 010 404/IC 010 404—DIGITAL ELECTRONICS (AI, EC, EI, IC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Explain the properties of Hamming codes. Mention its applications.
2. Define and explain : (i) Noise Margin ; (ii) Fan in ; (iii) Fan out.
3. What is the difference between combinational logic and sequential logic circuits ? Explain.
4. Mention the potential applications of flip flop. Explain any two in detail.
5. Draw the block diagram of PAL and explain it.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain the principle of Duality with an example.
7. Explain the subfamilies of TTL in detail.
8. Differentiate latch from FFs. Explain the difference.
9. Explain the types of RAM in detail.
10. Define Hazard. Explain the types of Hazard in detail.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. (i) Explain : (a) Gray code ; (b) XS 3 code with examples.

    (ii) Explain hexa decimal and octal number system with examples.

Or

Turn over

12 (i) Explain the limitation of K map.

(ii) Simplify the Boolean expression F = 1,4,5,9,12,14. Realize the simplified expression using only NAND gates.

13. (i) Explain positive and negative logics in detail.

(ii) Draw a TTL logic circuit with totem pole and explain it in detail.

Or

14. Explain the characteristics of TTL and CMOS logic families in detail.

15. Explain the half and full adders with schematic diagrams. Realize them with basic gates.

Or

16. (i) Explain all the types of FFs with diagrams, truth tables and excitation tables.

(ii) Derive the characteristic equations of all the types of FFs.

17. Draw a Binary ripple counter and explain it in detail. Bring out its design procedure.

Or

18. (i) Explain the bidirectional shift registers with a neat diagram.

(ii) Give an account on "Universal Register".

19. (i) Explain the steps to design a hazard free combinational circuit with an example.

(ii) Draw the architecture of GAL and explain in detail.

Or

20. (i) Draw the architecture of FPGA and explain it in detail.

(ii) Write a technical note on "Configurable PAL".

(5 × 12 = 60 marks)