

F 2992

(Pages : 2)

Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, DECEMBER 2012

Third Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 305 }
IT 010 304 } SWITCHING THEORY AND LOGIC DESIGN (CS, IT)

(New Scheme—Regular/Improvement/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Answer **all** questions.

Part A

Each question carries 3 marks.

1. State the different types of hazards.
2. What are Universal Gates ?
3. State the advantages of Parallel Adders.
4. Draw the circuit of D-Flip-Flop using NAND gates.
5. State and prove DeMorgan's Theorem.

Part B

Each question carries 5 marks.

(5 × 3 = 15 marks)

6. Convert the following binary numbers to its equivalent decimal numbers :

(a) 1101.

(b) 1011.

(c) 0.001101.

(d) 0.1101.

(e) 111011.101.

7. Explain the characteristics of CMOS gates.
8. Explain Carry Look Ahead Adder.
9. What is Race Around Condition ? How is it eliminated ?
10. Explain the working of Johnson counter.

(5 × 5 = 25 marks)

Part C

Each full question carries 12 marks.

11. (a) Design a BCD to excess 3 code converter.

(12 marks)

Or

- (b) Simplify using K map :

(i) $A(\bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C})$.

(6 marks)

(ii) $F(w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

(6 marks)

Turn over

12. (a) Explain with neat Figure (i) a Carry Save Adder ; (ii) Serial Adder. (6 + 6 = 12 marks)

Or

- (b) (i) What is PLA ? Explain. (6 marks)
 (ii) Compare PLA and PAL. (6 marks)

13. (a) Explain in detail, with a neat figure, the working of Master Slave JK Flip-Flop. (12 marks)

Or

- (b) A sequential circuit has 2 flip-flops A and B, 2 inputs x and y and an output z . The flip-flop input functions and the circuit output function are as follows :

$$J_A = xB + y'B' ; \quad K_A = xy'B'$$

$$J_B = xA' ; \quad K_B = xy' + A$$

$$Z = xyA + x'y'B$$

Obtain the logic diagram, state table, state diagram and state equations.

(12 marks)

14. (a) Explain the different types of Shift Register and their applications.

(12 marks)

Or

- (b) Design an asynchronous binary 4-bit up counter.

(12 marks)

15. (a) Write brief notes on the following logic families :

(i) TTL.

(ii) ECL.

(6 + 6 = 12 marks)

- (b) (i) Write briefly on Fault tolerance in combinational circuits.

(6 marks)

- (ii) Explain the different type of hazards in detail.

(6 marks)

[5 × 12 = 60 marks]